14.5 A DSSS UWB Digital PHY/MAC Transceiver for Wireless Ad hoc Mesh Networks with Distributed Control

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Wireless personal area network systems (WPANs) utilizing ultra-wideband (UWB) communication have been studied and proposed for wireless networking of consumer electronics products [1] [2]. Such systems are capable of high data rate transmission that exceeds several hundred Mb/s, and low power consumption. These systems commonly adopt a star topology composed of one control terminal and several user terminals, in which only the control terminal can manage the wireless network, as can be seen by an access point in WLANs. Wireless ad hoc mesh network systems (WAMNs) with distributed control, on the other hand, allow each terminal to have a network control function and configure its own optimal network according to local circumstances [3].

A direct sequence spread spectrum (DSSS) UWB digital PHY/MAC transceiver chip is presented which is equipped with a DSSS UWB PHY baseband circuit and a MAC circuit that performs the above-mentioned distributed control (herein after referred to as "PHY/MAC chip"). Our chipset consists of the above PHY/MAC chip, the previously reported RF chip [4], and "data link control (DLC) + CPU" chip which is equipped with data link control functions in 0.18μm CMOS [5]. In this paper, the functionality and performance of the PHY/MAC chip, the core of the chipset, are described in detail.

Figure 14.5.1 shows the block diagrams of the PHY/MAC chip and the system utilizing it, and the physical-layer packet format. "DSSS UWB PHY" and "distributed control MAC" functions are implemented in a die area of 12.2 mm^2 in a 0.13μm CMOS process.

Data input from the DLC+CPU chip is delivered to the TX packet assembler, where a PHY data payload is generated and a PHY header is appended. The data are then FEC-encoded (convolutional code (R=1/2) + Reed-Solomon code (224,240)), have a preamble appended, and are DSSS-modulated, generating the physical-layer packet illustrated in Fig. 14.5.1. The DSSS circuit performs spreading modulation for this packet at 1Gchip/s of chip rate. The spreading factor for payloads can be selected from 1, 2, 4, and 8, allowing PHY data rates of 1000, 500, 250, and 125Mb/s (466, 233, 116, and 58Mb/s with FEC redundancy). After DSSS modulation, TX signals are divided into TXI and TXQ on a chip by chip basis and outputted to the RF chip [4], where π/2 shift BPSK is performed at the TX pulse modulator.

Figure 14.5.2 shows the receiver block diagrams and the preamble format. RX signals are divided into Ich and Rch signals at the quadrature demodulator in the RF chip and go through the LPFs and the AGCs. The signals are then processed with a 2b ADC at a 1GHz sampling rate, respectively, and inputted to the PHY/MAC chip together with the 500MHz clock. PHY processing is performed with the 125MHz clock obtained by dividing the 500MHz clock by 4 in the PHY/MAC chip, thus achieving 1Gchip/s by 8-parallel data processing.

The preamble portion (8064ns) consists of 128-chip spreading codes in certain repetition patterns. By exploiting this structure, our newly developed coherent channel measurement (CCM) is performed. We achieved fast acquisition within 8064ns and RAKE path searching at the same time by using CCM, thus it has an advantage of circuit simplicity compared with other UWB systems which use both DSSS and RAKE methods. Figure 14.5.3 shows the block diagram of the CCM circuit. Using 32 correlators for one clock, each of which performs despreading of 8chips, 128point (128ns) wireless channel data are obtained with 1ns resolution in 640ns. Then, RF clock phase control signals are delivered from the PHY sequence controller to the RF chip, and the phase of the RF clock is rotated by 180 degrees, followed by the same channel measuring technique described above. This phase control enables variable ADC sampling timing in the RF chip, leading to 500ps resolution. Thereafter, phase inversion and CCM are repeated by turns and measurement data for 0 degree and 180 degrees are moving averaged, respectively. Then, the preamble end pattern is detected by judging whichever one has the higher level. After detecting a preamble, RAKE combination is performed based on the CCM data, and the received symbols are demodulated and FEC-decoded. The PER performance for each data rate is shown in Fig. 14.5.4. Deviation from the simulation values, attributed to RF chip performance and variances in pc board implementation, is less than 3.5dB at 1% of packet error rate.

Exploiting the resolution of 500ps, the PHY/MAC chip is capable of measuring a range between two terminals with the hardware capability of ±7.5cm distance resolution. The ranging data is used for knowing the position of each terminal node (TN) for selecting a good routing path on our WAMNs. The right side of Fig. 14.5.4 shows the ranging performance in a line-of-sight condition. We obtained ±3cm accuracy of ranging within 5m; this is done by repeated measurement and statistical processing by software.

The PHY/MAC chip realizes distributed control based on the 40ms time window called a "super frame (SF)." Figure 14.5.5 shows that each terminal node transmits a beacon every 40ms and receives beacons from other TNs during that period. Target beacon transmission time (TBTT) is the timing when each TN transmits a beacon. The TBTT interval is 625μs so that 64TNs can be accommodated within 40ms. The TBTT interval has two control periods: transmit guaranteed period (TGP) and fair access period (FAP). The TGP is the period in which the beacon-transmitting TN is given priority to transmit data. During the FAP, on the other hand, any TN is allowed to transmit. A beacon includes not only the TN's own TBTT information but also neighbor TNs' TBTT information which enables each TN to obtain TBTT information of all TNs in the entire system. Since other TNs' TGP timing is known to each TN, collision is avoided. Thus, distributed control of up to 64 terminals is realized without an access point. Figure 14.5.5 shows a block diagram of the access controller, the core block of the above-mentioned distributed control. No previous work has achieved implementation of such distributed control for WPANs.

Figure 14.5.6 shows the specification and performance summary of the PHY/MAC chip and Fig. 14.5.7 shows the die micrograph. The die size is 4.9×4.9mm^2, 51% of which is utilized for the logic occupying 12.2mm^2.

References:

[1] E. Fujita et al, http://grouper.ieee.org/groups/802/15/pub/2003/May03, 03138r2P802-15, 10-May-2003.
[2] http://www.ieee802.org/15/pub/TG3a.html, May, 2005.
[3] Shugong Xu and Tarek Saadawi, "Does the IEEE 802.11 MAC Protocol Work Well in Multihop Wireless Ad hoc Networks?," *IEEE Communications Magazine*, pp. 130-137, June, 2001.
[4] S. Iida, et al, "A 3.1-5GHz CMOS DSSS UWB Transceiver for WPANs," *ISSCC Dig. Tech. Papers*, pp. 214-215, Feb., 2005.
[5] Shin Saito, et al, "Wireless (UWB) Multi-hop CE Network Demonstration," *IEEE CCNC2006*, Jan., 2006.

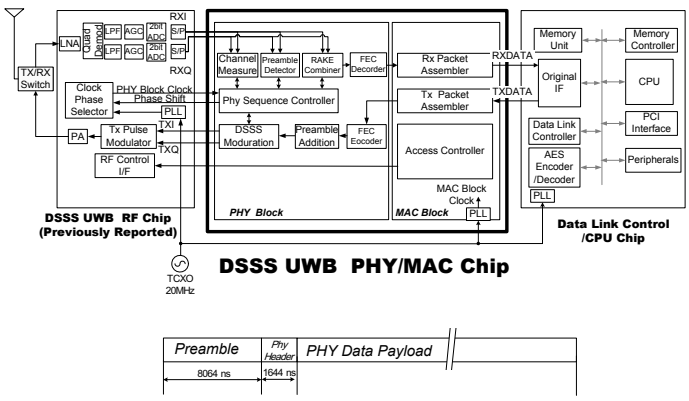

Figure 14.5.1: System block diagram and physical-layer packet format.

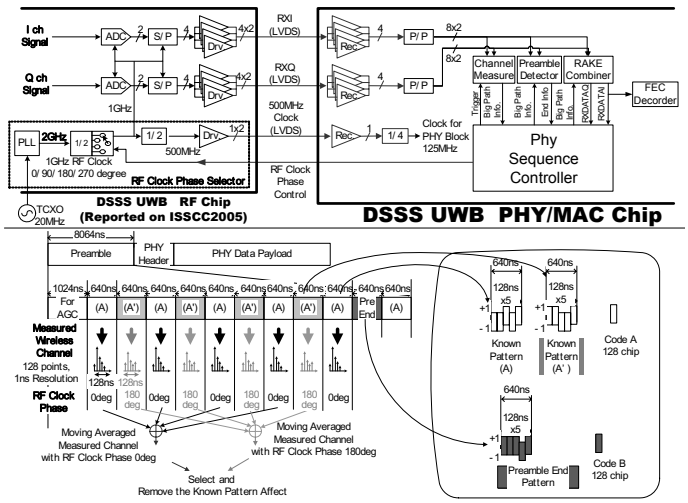

Figure 14.5.2: Receiver block diagrams and preamble format.

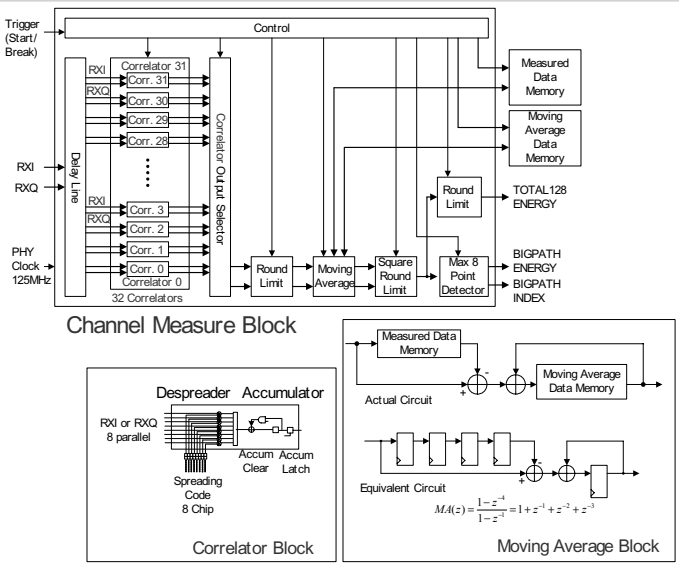

Figure 14.5.3: Block diagrams of coherent channel measure block.

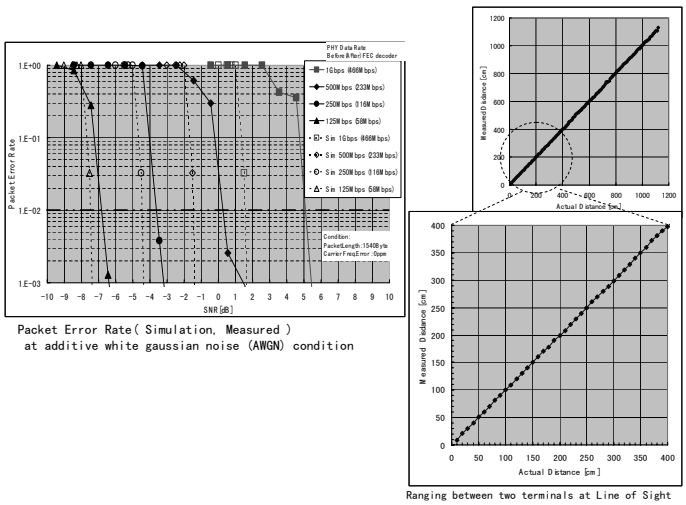

Figure 14.5.4: Performance results (packet error rate, ranging).

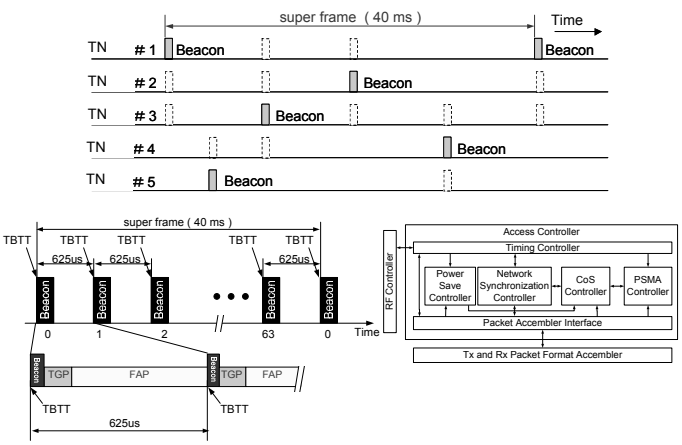

Figure 14.5.5: Distributed media access control mechanism.

Chip Specification	Modulation	π/2 shift BPSK + DSSS
	Forward Error Correction (FEC)	Convolutional code(R=1/2) + Reed-Solomon code(224, 240)
	Spread Spectrum Chip Rate	1Gchip/s
	PHY Data Payload Spreading Factor	1, 2, 4, 8
	PHY Data Rate (without FEC) [bps]	1000M, 500M, 250M, 125M
	Data Rate [bps]	466M, 233M, 116M, 58M
	Number of RAKE path / Resolution	1 to 8 / 1ns
	Ranging Accuracy [cm]	+/- 7.5
	Access Method	Preamble Sense Multiple Access(PSMA)
	Number of terminal with Distributed Control	up to 64
Process Technology	Technology	0.13μm CMOS
	Die Area of Core Logic Block	12.2 mm^2
	Supply Voltage	Core 1.2V / IO 3.3V
Performance Summary	Measured Ranging Accuracy with statistical work in Software [cm]	+/- 3 (< 5m, line of sight) +/- 5 (< 12m, line of sight)
	Acuisition Time [nsec]	< 8064
	Maximum Throughput [Mbps]	303 (network mode) / 378 (peer to peer mode)
	Power Consumption of 1.2Volt Core Block [mW]	181 (max.) / 45 (min.)

Figure 14.5.6: Chip specification and performance summary.

Continued on Page 652

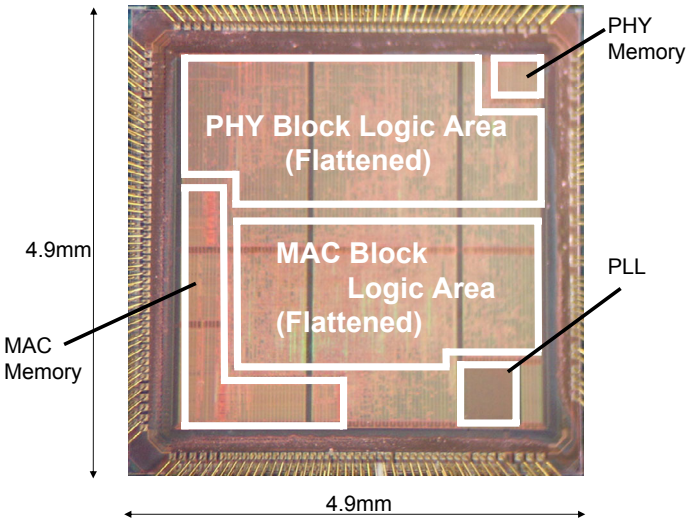

Figure 14.5.7: Die micrograph.

